Application No. 10/614,503
Office Action: mailed Aug 13, 2004
Amndt. dated: Oct 30, 2004

REMARKS/ARGUMENTS

Claims 21, 22, 24-26, 28 and 29 have been amended; no claims have been cancelled and no new claims have been added. Claims 21-39 are pending in this application.

The allowance of claims 31-39 has been noted with appreciation.

Claim rejections under 35 US 102(e)

Claims 21-23 and 25-27 were rejected as anticipated by US Patent 5,218,704 (Watts, Jr.). (It is noted that Watts, Jr. 6,397,340 issued on an application which is a continuation application related back to Patent No. 5,218,704 relied on in the previous Office Action.)

To anticipate a claim under 35 US 102, a reference must disclose each and every feature as recited in the claim under rejection. Watts Jr. fails to meet this standard in relation to claims 21 and 25 as presented by in this response because Watts Jr. does not disclose: "monitoring a time related level of processing activity by a processing unit including a processor by counting processor operation events over a predetermined time interval" as recited in claim 21, or "monitoring a time related level of processing activity by a processing unit by counting over a predetermined time interval events associated with processing operations by the processing unit", as recited in claim 25. In contrast, Watts, Jr. discloses at col. 6, lines 4-7 "the period of time between service requests can be used to determine the activity level of any application software running on the computer and to provide slice counts for power conservation. . .". The feature of claim 18 of Watts, Jr. relied on by the Examiner (at col. 13, lines 55-56), is an ambiguous and unclear recitation: "a processor having a monitor for measuring the relative amount of activity time within said processor" that does not correspond to the above recitations in claims 21 and 25, respectively. Claims 21 and 25 are not anticipated by Watts, Jr. and are supported by disclosure in the specification at least in paragraphs [0010] and [0018]. Claims 22 and 26 include amendments for antecedent consistency with their parent claims. It is urged that claims 21-23 and 25-27 are in condition for allowance.

Claim rejections under 35 USC 103

Claims 24 and 28-30 were rejected under 35 US 103(a) as unpatentable over US Patent 6,397,340 (Watts Jr.) in view of US Patent 4,670,837 (Sheets). The rejection is respectfully

traversed. The Examiner asserts that Sheets teaches a feature "wherein the processor activity is determined by monitoring access by the processor to memory coupled to the processor", citing to Sheets col. 2, lines 7-29 and col. 3, lines 1-4. Those passages appear to be directed to implementing memory and I/O read and write operations, not to monitoring operations, and Sheets states: . ."Reducing the clock frequency reduces the power consumed by microprocessor 101 and, by reducing the required access rate to the associated devices, i.e., ROM 107, RAM 108, and I/O port 109, also reduces the power consumed by those devices." (col. 2, line 68 – col. 3, line 4). Considering each of Watts, Jr. and Sheets in its entirety (see MPEP 2141.02), Sheets also appears to conflict with the teaching of Watts, Jr., that "the period of time between service requests can be used to determine the activity level of any application software running on the computer and to provide slice counts for power conservation . . ." (Col. 6, lines 1-9). Consequently, modification of Watts, Jr. by Sheets as proposed by the Examiner cannot be obvious – see MPEP 2143.01. Sheets is not seen to disclose or to suggest "monitoring a time related level of processor activity in a CPU by counting over a predetermined time interval, processor operation events involving selected memory access operations, and increasing or decreasing the CPU processor performance level according to the monitored level of processing activity compared with a reference level." in the context of claim 28, nor to disclose or suggest "wherein the processor activity is determined by counting accesses by the processor to memory coupled to the processor" as recited in claim amended 24 considered in conjunction with its parent claim 21. Claims 24 and 28-30 are patentable over Watts, Jr. in view of Sheets.

It is believed that all pending claims are in condition for allowance and early action to that effect is solicited. If there are any issues that could be resolved by discussion, a telephone call to the undersigned attorney at (972) 862-7428 would be appreciated.

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Respectfully submitted,

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